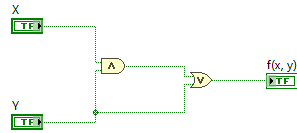
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Section 19

Cpr E HW 01

1. Define the following terms in no more than 2 sentences each
   1. CAD – Computer Aided Design: The use of computers in aiding or creating designs.
   2. PCB – Printed Circuit Board: Supports and electronically connects electronic components
   3. PLD – Programmable Logic Device: An electronic component used to build reconfigurable digital circuits
   4. FPGA – Field Programmable gate array: An integrated circuit table configured by a customer or designer after manufacturing, hence the “field.”
2. In the development process initial design-simulation-verification is one loop and prototype implementation-testing-verification is another loop. Answer the following in 4-5 Sentences:
   1. Which look is relatively more expensive, and why?
      1. I would say that the **prototype implementation-testing-verification loop** would be more expensive. It would cost a lot of money to design and produce a physical copy of a prototype, then take lots of time to manually test it in-person, as well as human error being a more prevalent factor. When designing and simulating a product on a computer, the simulations can be run on a separate device while other work can be done, as well as there being no error in simulations as the computer would perform them exactly how they were programmed to.
   2. Can any of these loops be avoided? If not, why not? If yes, what’s the penalty?
      1. These two loops are very important, and not using them would cause more penalty than gain, mainly being that you’d have to use another strange system that wouldn’t work as well as these. I think that these two methods are essential because they represent the 2 best ways of formulating a product. These are the 2 best and most efficient ways of doing so compared to the other methods.
3. Convert the Following Numbers to Decimal:
   1. 11110102 – 122
   2. 10112 – 11
   3. 11108 – 584
   4. 111116 – 4369
   5. BEE16 – 3054
4. Convert the following numbers to binary
   1. 43 – 101011
   2. 101 – 1100101
   3. 281 – 1000011001
   4. 38116 – 1110000001
   5. BEEF16 – 1011111011101111
5. Consider the following statement: “If any of my two friends picks me up in time and the movie is not sold out or my friend who picks me up has already bought me tickets then I will see the movie tonight.” Suppose the events that your two friends pick you up on time are represented by logic variables A and B respectively, for the two friends; Their having bought tickets in advance are represented by logic variables T1 and T2, respectively; the movie being sold out is represented by the logic variable S, then write down all combinations of logic variables (like X=1 and Y=0) one at a time, which when true will allow you to see the movie.
   1. ((A + B) • !S) + (A • T1) + (B • T2)
6. Consider the logic function f(x, y) = y + (x • y).
   1. A. Draw the circuit diagram for f(x, y).
      1. 
   2. Write down the truth table for f(x, y).

|  |  |  |
| --- | --- | --- |
| x | y | f(x, y) |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

* 1. By looking at the truth table in (B), what observation can you make about f(x, y)?
     1. I observed that the function only returns a 1 value when only 1 of the values is 1. When both are either 1 or 0, the function returns a 0.

1. Consider the circuit below. Name the 3 inputs as A, B, C, and the output as F.
   1. Write the logic expression for it.
      1. ((!A • B • C) + (!A • B • !C) + (A • C)) = F
   2. Write the truth table for the circuit.

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | F(A, B, C) |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

1. Consider the circuit below.
   1. Write the logic expression for the output F.
      1. A + (B • C) + !D
   2. Write the truth table for the circuit.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | F(A, B, C, D) |
| 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |